REMARKS

The application was filed on 10 September 1999 with twenty-one claims. The Examiner, on 03 October 2002, first rejected claims 4-7, 17, 16 and 19 under 35 U.S.C. §112; claims 19 and 20 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,385,708 entitled *USING A TIMING-LOOK-UP-TABLE AND PAGE TIMERS TO DETERMINE THE TIME BETWEEN TWO CONSECUTIVE MEMORY ACCESSES* to Stracovsky et al. (Stracovsky '708); and claims 1-21 under 35 U.S.C. §103(a) as being unpatentable over Stracovsky '708 in view of U.S. Patent No. 6,088,772 entitled *METHOD AND APPARATUS FOR IMPROVING SYSTEM PERFORMANCE WHEN REORDERING COMMANDS* to Harriman et al. (Harriman '772). Applicants revised the specification and amended claims 1, 16, 17, and 19 to remove rejections under 35 U.S.C. §112. Applicants traversed the rejection of the claims based on the art of Stracovsky '708 alone and in combination with Harriman '772. Applicants submitted formal drawings. The Examiner finally rejected claims 19 and 20 under Stracovsky '708, and claims 1-18, 21 under Stracovsky '708 and Harriman '772. Applicants attempted to amend the claims to put them in condition for allowance and/or in better condition for appeal, but the amendments were not entered.

On 23 July 2003, Applicants filed a Request for Continued Examination. The Examiner then issued a new rejection of claims 19 and 20 under 35 U.S.C. §103(a) over Stracovsky '708 and U.S. Patent No. 6,601,151 entitled Apparatus and *METHOD FOR HANDLING MEMORY ACCESS REQUESTS IN A DATA PROCESSING SYSTEM* to Harris (Harris '151), but still maintains the original rejection of claims 1-18 and 21 under 35 U.S.C. §103(a) over Stracovsky '708 and Harriman '772.

Applicants maintain their traversal of the rejections because there is no basis in fact for the combination of Stracovsky '708 with Harriman '772 or with Harris '151. Claims 1-21 are pending.

The Rejection Under 35 U.S.C. § 103(a) over Stracovsky '708 and Harriman '722

The Examiner rejected claims 1-18 and 21 as being obvious in view of Stracovsky '708 in view of Harriman '722. Stracovsky '708 proposes a universal memory controller between multiple processors and multiple memories wherein the controller has a circuit designed to specifically avoid data transfer collisions of memory commands. Stracovsky '708 issues a command to memory only when its command issue time is zero. The value of the command issue time relates to the most recent memory command corresponding to the same logical bank in memory, i.e., the value of the command issue time for a particular command indicates the latency between two commands to the same bank and is determined largely by the physical characteristics of the memory. The command issue time, moreover, is decremented once per clock cycle irrespective of command type unless commands are to the same memory bank. Given one command with a command issue time of zero, Stracovsky '708 will not allow another command to the same bank to issue until the first command is issued. Thus, if the command issue time for a command directed to a particular bank reaches zero and if the command has not issued, the command issue time for all other commands to the same bank cannot be decremented until the first command is issued. Stracovsky '708 allows a command to issue only if its command issue count is zero and there are no collisions on the data bus indicated.

Harriman '722 teaches a memory access controller in which memory commands are first separated into queues depending on the type of command and then the commands to the same memory portion are fenced and allowed to execute up to a fence count of a number of quadwords. Harriman '722, thus, teaches that it is favorable for sequential commands to access the same portion of memory and does not consider the least memory cycle performance penalty when reordering and grouping commands. Harriman '722 simply groups those

commands that access the same page of memory and then fences the commands for execution.

Despite the Examiner's creative hindsight and assertion that the alleged combination would result in increased memory access efficiency by improving overall locality of reference and/or command type and balancing latency and bandwidth concerns, Applicants maintain there is no suggestion or motivation to combine Stracovsky '708 with Harriman '722. Harriman '722 teaches a method to access a same portion of memory for time determined by a fence count of quadwords. Stracovsky '708 teaches a method to avoid data collision and is concerned with memory latency but only to the extent that those collisions must be avoided. Stracovsky '708 allows those commands having a command issue time of zero to execute, irrespective of command type, and irrespective of location unless the commands are to same memory bank, in which case the subsequent commands cannot issue. So, herein lies the inherent contradiction between Stracovsky '708 and Harriman '722 and the reason why the two references cannot be combined! Stracovsky '708 will not issue two commands to the same bank while Harriman '722 teaches it is preferable to issue multiple commands to the same bank. A practical reason, exists, moreover for this apparent contradiction. Because Stracovsky '708 deals with very large computer systems having multiple processors accessing large memory, it is highly unlikely and almost certain that no two commands will access the same memory bank. On the other hand, Harriman '722 teaches that its system is compatible with the Accelerated Graphics Port (AGP) wherein graphics data is most likely stored in the same memory page or in very close proximity. Given the above considerations, one of skill in the art would not be inclined to combine Stracovsky '708 which prohibits commands to the same bank from issuing until the oldest command issues in order to avoid data

transfer collisions with Harriman '772 which prefers accessing the same memory portion to access graphics data.

Applicants respectfully request the Examiner to withdraw the rejection of claims 1-18 and 21 based on the combination of Stracovsky '708 and Harriman '772 because Harriman '772 teaches sequential accesses to the same memory bank whereas Stracovsky '708 teaches that accesses to the same memory bank are to be avoided because they may result in data transfer collisions. In any event, the combination does not teach reordering commands in command queues based on least memory performance penalty, as claimed.

The Rejection Under 35 U.S.C. § 103(a) over Stracovsky '708 and Harris '151

The Examiner rejected claims 19 and 20 under 35 U.S.C. §103(a) under the combination of Stracovsky '708 and Harris '151 alleging that Stracovsky '708 teaches all the claimed elements except for a plurality of comparison logic circuits, each associated with one of a plurality of command FIFO queues. The Examiner reasons that system efficiency would be improved by providing separate queues and associated logic blocks for reads and writes so that the logic blocks can be tailored specifically to the memory access request type, per Harris '151.

Stracovsky '708 is described above with respect to the earlier rejection. Harris '151, on the other hand, describes a memory controller to increase the throughput of memory access requests in a data processing system, **independent of memory access times and memory bandwidth.** (Harris '151 at column 1, lines 46-50). The combination of Stracovsky '708 with Harris '151 is a combination that achieves the same result: avoidance of data collision. Harris '151 at column 2, lines 34-26 states that the comparison logic can reorder commands so that a memory access can be suppressed if there is an earlier memory access request still being serviced by the data storage element

of the kind which would prevent the servicing of the later memory access request.... and then at column 2, lines 55-59 teaches preferential transmission of a memory access request which have address portions that do not match the memory access request-type portions of any of the list entries. The comparison logic is not one to determine which memory commands have the least memory cycle performance penalty, as claimed in claim 19. The comparison logic of Harris '151 is nothing more than an address dependency check, indicated to be separate from the memory cycle performance penalty. There is no suggestion in either Harris '151 nor Stracovsky '708 that combining comparison logic that checks do address dependency is the same as comparison logic that determines the least memory cycle performance penalty. Stracovsky '708 has a complicated system involving a command issue time which is decremented to avoid collisions on a multibus, multimemory, multiprocessing system. Merely adding address dependency checking does not improve any performance resulting from evaluation and reordering of commands based on memory cycle performance.

Applicants request the Examiner to reconsider and withdraw the rejection of claims 19 and 20 under Stracovsky '708 and Harris '151. If, however, the rejection is maintained, Applicants further request the Examiner to particularly state where the suggestion to combine the references exists and how the combination results in comparison logic to determine the least memory cycle performance penalty, as claimed in claims 19 and 20.

Conclusion

Applicants still maintain that Stracovsky '708 and Harriman '772 cannot be combined because of the nature of the different computer systems, i.e., Stravosky '708 is a large multiprocessor, multimemory system handling different requests to different memory banks and Harriman '772 discloses a

graphic memory controller where it is highly likely the requested data will be in the same memory bank. Stracovsky '708, moreover, is not concerned with command type, only with avoiding data collisions which will most likely result when memory commands to the same memory portion are issued. Harriman '772, on the other hand, has created a memory controller especially to access the same portion of memory.

Applicants have reviewed U.S. Patent 6,363,466 entitled *INTERFACE AND PROCESS FOR HANDLING OUT-OF-ORDER DATA TRANSACTIONS AND SYNCHRONIZING EVENTS IN A SPLIT-BUS SYSTEM* to Anand (Anand '466) and do not consider it to be prior art. Applicants thus respectfully request the Examiner to reconsider the application in view the amendments and the remarks, and pass the application to issuance. The Examiner is further invited to telephone the Attorney listed below if he thinks it would expedite the prosecution and the issuance of the patent. In fact, upon receipt of this response, Attorney for Applicant requests a telephone interview to further understand the Examiner's point of view.

Respectfully submitted,
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